REMARKS

Claims 1, 3-7, 9-12 and 14-23 are pending in the Application, of which Claims 16-20 are withdrawn from consideration and Claims 21 and 22 are presently cancelled. The Examiner objected to earlier amendments to Claims 1, 7 and 23, and rejected Claims 1, 3-7, 9-12 and 14-23. Claims 1, 7 and 23 are amended by this Response.

Response to Office Action

I. 35 U.S.C. § 132 -- New Matter [OA ¶ 1]

The Examiner objected to the amendments filed on May 29, 2001 under 35 U.S.C. § 132 stating that the amendments added new matter. The Examiner makes four objections relating to Claims 1, 7 and 23.

Objection [1] - Claim 1: "depositing an insulator layer of high temperature oxide ***directly*** on *the substrate*"

The Examiner objects to the language "depositing an insulator layer of high temperature oxide directly on the substrate" of Claim 1. The present Response introduces a clarifying amendment that replaces "[the substrate]" with "exposed portions of the tunnel oxide layer." Therefore, Claim 1, as amended, recites "depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer."

Support for " an insulator layer of high temperature oxide" is found, e.g., in the Specification at page 4, lines 22-24, which states "Insulator 30 is preferably a high quality oxide which will prevent charge from leaking out vertical side surfaces 17 of floating gate 16. High temperature oxides, such as a LPCVD furnace grown oxide, are high quality oxides."

Support for "directly on the substrate," which is presently amended to "directly on the exposed portions of the tunnel oxide layer," is found, at least in the Summary and the Drawings. In objecting to "directly on the substrate," the Examiner states that "the specification only shows *depositing an insulator **on the substrate, NOT directly on***." Additionally, the Examiner states that "figure 5 of the instant application only shows the insulator 30 is directly on the tunnel oxide layer 14." (OA of August 9, 2002 at page 13,

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paragraph 11.) Applicants agree with the Examiner that Figure 5 of the instant Application shows at least the insulator directly on the tunnel oxide layer.

Therefore, the Specification supports the amended Claim recitation of "depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer." No new matter is added by the amendments to Claim 1.

Objection [2] - Claim 1: "the insulator layer forming *sidewalls around the floating gate*"

The Examiner objects to the language "the insulator layer forming sidewalls around the floating gate" of Claim 1. The present Response amends Claim 1 to recite "the insulator layer forming around vertical surfaces of the floating gate to prevent charge leaking from the floating gate."

The recitation "the insulator layer" has support in the Specification at least as described above in Objection [1].

The recitation "forming around vertical surfaces of the floating gate" is supported by the Specification. In objecting to Claim 1, the Examiner states "the specification only shows forming the insulator on both sides of the floating gate, **NOT** sidewalls around the floating gate." (OA of August 9, 2002 at page 13, paragraph 11.) The Specification discloses an insulator forming an insulator on each vertical surface of the floating gate, not simply two ("both") sides of the floating gate as the Examiner states. Though the Figures 5-7 show an insulator 30 abutting two vertical side surfaces 17 of the floating gate 16, a cross sectional drawing could only show two sides of a three-dimensional object without obstructing the view. Additionally, the Specification discloses that "The floating gate has a plurality of vertical surfaces ... The memory cell further includes **an insulator** disposed on the tunnel oxide and **abutting the plurality of vertical surfaces of the floating gate**. The insulator is formed by first depositing a layer of the insulator on the substrate." (Specification, page 2, lines 28-31.) The Specification does not disclose forming an insulator on only two of the vertical surfaces but discloses forming an insulator on "the plurality of **vertical surfaces of the floating gate**." Forming an insulator that abuts the plurality of vertical surfaces of the floating gate supports "forming around vertical surfaces of the floating gate."

The recitation "to prevent charge leaking from the floating gate" also has support in the Specification, which states, e.g., "Insulator 30 is preferably a high quality oxide which

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will **prevent charge from leaking out vertical side surfaces** 17 **of floating gate** 16." (Emphasis added, Specification, page 4, lines 22.)

Therefore, the Specification supports the Claim recitation of "the insulator layer forming around vertical surfaces of the floating gate." No new matter is added by the present amendments to Claim 1.

Objection [3] - Claim 7: "deposing an insulator layer on high temperature oxide *directly on the tunnel oxide*"

The Examiner objects to the language "deposing an insulator layer on high temperature oxide directly on the tunnel oxide" of Claim 7. The present Response amends Claim 7 to clarify that "depositing an insulator" is directly on exposed portions of the tunnel oxide layer. Therefore, Claim 7, as amended, recites "depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate."

With regard to "insulator layer" and "high temperature oxide," see Objection [1] above.

With regard to "directly on exposed portions of the tunnel oxide layer," the Examiner states that "it is noted that only portions of the insulator layer of high temperature oxide is *directly on the tunnel oxide*." (OA, page 2, paragraph 1.) Claim 7 recites both "the tunnel oxide layer **and the floating gate**" not just "*the tunnel oxide.*" Applicants again point out that the Examiner recognizes that "figure 5 of the instant application only shows the insulator 30 is directly on the tunnel oxide layer 14." (OA of August 9, 2002 at page 13, paragraph 11.) As discussed above the insulator layer is formed directly on the substrate having a tunnel oxide layer. Similarly, the insulator layer as shown in the Drawings is also formed directly on the exposed portions of the floating gate.

Therefore, the Specification supports the Claim recitation of "depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate." No new matter is added by the amendments to Claim 7.

Objection [4] - Claim 23: "the insulator layer forming *sidewalls of high quality oxide around the floating gate*"

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The Examiner objects to the language "the insulator layer forming sidewalls of high quality oxide around the floating gate" of Claim 23. Claim 23 is presently amended to recite "the insulator layer of high quality oxide on the vertical surfaces around the floating gate to prevent charge leaking from the floating gate."

Support for "the insulator layer ... on the vertical surfaces around the floating gate" is found in Objection [2] above.

Support for "of high quality oxide" is found at least in the Specification at page 4, line 22, which states "**Insulator 30 is preferably a high quality oxide**."

Reconsideration and withdrawal of all the § 132 objections are requested.

II. 35 U.S.C. § 112 -- Claim Rejections [OA ¶¶ 2-3]

The Examiner rejected Claims 1, 3-7, 9-12, 14-15 and 21-23 under 35 U.S.C § 112, first paragraph, as containing subject matter that was not described in the Specification. As discussed above, the Specification supports the amendments made to Claims 1, 7 and 23. Thus, Claims 1, 3-7, 9-12, 14-15 and 21-23 do not contain new subject matter. Reconsideration and withdrawal of the § 112, first paragraph rejections are requested.

III. 35 U.S.C. § 102(b) -- Claim Rejections [OA ¶¶ 4-5]

The Examiner rejected Claims 1, 5, 7 and 11 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,713,142 ("Mitchell"). The Examiner states:

> [5.] Mitchell et al. discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layers, to provide a floating gate 33 (fig. 2a); depositing an insulator layer of oxide 37 (CVD oxide, inherently shows the oxide is the high temperature oxide) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layers, see figs. 1-5, cols. 1-6.

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Claim 1

Mitchell does not teach depositing an insulator directly on the floating gate. Claim 1 recites "**depositing an insulator** layer of high temperature oxide **directly on** exposed portions of the tunnel oxide layer and **the floating gate** . . . to prevent charge leaking from the floating gate." (Emphasis added). Hence Mitchell does not anticipate this part of Claim 1.

Mitchell does not disclose depositing an insulator to a thickness greater than the thickness of the floating gate. Claim 1 is further distinguished over Mitchell by reciting other features not disclosed or suggested by Mitchell. For example, according to Mitchell, neither the oxide layer 36 nor the insulator layer 37 is deposited to "a thickness greater than a thickness of the floating gate," as recited in Claim 1. As illustrated in Mitchell's figs. 2c and 2d, oxide layer 36 is a very thin layer formed over the floating gate and the thickness of insulator layer 37, at best, is substantially the same as the thickness of the floating gate. To the contrary, the Examiner states that Mitchell shows "polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer" as Claim 1 recites. Specifically, the Examiner states that:

> The Examiner disagrees because fig. 2C, layer 37 clearly shows this feature (the layer 37 having a thickness greater than the floating gate, for example, the thickness at both sides of the floating gate); furthermore, Mitchell et al. also states in col. 3, line 25-27, that the etch is continued until the surface of polysilicon layer 33 is exposed, which means in order to achieve the planar surface as shown in fig. 2d, the dielectric layer 37 must be etched in order to have the same thickness of the polysilicon layer 33, also see col. 4, lines 55-60.

The Examiner is relying on Mitchell's figures 2c and 2d disclosing that the gate oxide layer is greater in thickness than the floating gate layer. It is well known that when a reference does not explicitly disclose that the drawings are drawn to scale, arguments based on measurements of the drawing figures are of little value. See MPEP 2125. "[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue."[1] Here, Mitchell does not disclose that the figures are to scale and is completely silent as to the

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[1] *Hockerson-Halberstadt, Inc. v. Avia Group Int'l*, 222 F.3d 951, 956 (Fed. Cir. 2000).

particular heights of the layers. In fact, silicon dioxide layers 37 of Mitchell appears to be no higher than the top of polysilicon layer 33.

The Examiner also relies on Mitchell's claim 1. Mitchell's claim 1 does not imply "the insulator layer being deposited to a thickness **greater** than a thickness of the floating gate" as recited in Claim 1 (emphasis added). Mitchell's claim 1 is consistent with Mitchell's figures that show the insulator 37, when viewed at a point halfway between gates 33, is not greater than the thickness of the gate 33, but at best substantially even in height with gate 33. Mitchell clearly does not contain enabling disclosure that would convey to one skilled in the art the relevant feature of Claim 1, and therefore, does not anticipate this part of Claim 1.

Mitchell teaches using two insulators instead of a single insulator. With regard to layers 36 and 37, the Examiner states that the "Applicant further argues that the Mitchell et al. use two (36 and 37) separate insulator layers, *it is noted that the instant application also use two separate insulator layers as well (see page 4, lines 15-20).*" (OA, pages 14.) The Examiner correctly points out that the Specification discloses "an optional thermal oxidation" as well as "an insulator layer 30," however, the optional thermal oxidation is indeed optional and is not called for in Claim 1. Claim 1 does not recite "thermal oxidation," therefore, it is inappropriate for the Examiner to reject Claim 1 based on allegedly having "separate insulator layers." To the contrary, Mitchell's insulator layer 37 is formed directly over an oxide layer 36, wherein oxide layer 36 is the layer that enhances "charge retention of the floating gate" (Mitchell, col. 2, line 68 and col. 3, lines 1-3). Claim 1 is thus distinguishable over the cited reference additionally because Claim 1's single "insulator layer of high temperature oxide" accomplishes the same effect as the two separate layers 36 and 37 taught by Mitchell, so Mitchell also does not anticipate this part of Claim 1.

Mitchell teaches two separate steps to form an oxide layer 36 and an insulator layer 37 over a floating gate. Mitchell's figure 2b shows "thermal oxidation to form silicon dioxide layer 36." Mitchell's silicon dioxide layer 36 deposited on the substrate is not of a thickness that is greater than the first thickness as required by Claim 1. Mitchell then discloses an intervening step of "ion implantation." (Mitchell, col. 3, lines 3-8.) Next, Mitchell discloses forming a "thick silicon dioxide layer 37." (Mitchell, col. 3, lines 8-12.) Silicon dioxide layer 37 acts to insulate, whereas silicon dioxide layer 36 acts to enhance a "charge retention of the floating gate" (Mitchell, col. 3, lines 1-3). But, the method in accordance with

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Claim 1 advantageously involves only one step to form a high temperature oxide serving to both insulate and prevent charge from leaking.

During the telephonic interview of October 3, 2001, the Examiner indicated that Claim 1 of Mitchell (column 4, lines 53-55) teaches "depositing a conformal layer of insulating material on the surface of said substrate and said conductive strips." Applicants submit that the Examiner is taking that teaching out of context. If anything, Mitchell teaches away from the present invention. For example, at column 4, lines 60-62, Mitchell discloses "forming a layer of ***conductive material*** on the surface of said conformal layer" (emphasis added). In contrast, Claim 1 recites "depositing a ***dielectric*** layer on the planar surface" (emphasis added). Since a dielectric layer is NOT conductive, Mitchell when read in its entirety, teaches away and is patentably distinguishable from Claim 1.

Thus, for all the above reasons, Applicants request reconsideration and allowance of Claim 1.

Claim 5

Claim 5 depends on independent Claim 1. For at least the reasons stated above for the allowance of Claim 1, dependent Claim 5 is also allowable. Applicants request reconsideration and allowance of Claim 5.

Claim 7

Applicants respectfully submit that Mitchell does not teach or suggest that "depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate such that the insulator layer has a thickness that is greater than the first thickness," as recited in presently amended Claim 7. Mitchell deposits layer 37 directly on layer 36 and not directly on the tunnel oxide layer 32. Claim 7 recites "depositing a floating gate layer on the tunnel oxide." Claim 7 also recites "depositing an insulator ... directly on exposed portions of the tunnel oxide layer," the same tunnel oxide. Mitchell discloses two layers (32 and 36), which the Examiner misconstrues as the same layer. The layer 36, which Mitchell deposits an insulator 37, is not the layer that Mitchell deposits on the floating gate 33. Mitchell's gate 33 is deposited over 32 and is under layer 36. For substantially the reasons stated above with respect to Claim 1, Claim 7 as amended and thus its dependent Claim 11 are each allowable over the cited prior art.

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Claim 11

Claim 11 depends on independent Claim 5. For at least the reasons stated for the allowance of Claim 5, dependent Claim 11 is also allowable. Applicants request reconsideration and allowance of Claim 11.

Thus, for the above reasons, Applicants request reconsideration and withdrawal of this rejection of Claims 1, 5, 7 and 11.

IV. 35 U.S.C. § 102(e) -- Claim Rejections [OA ¶ 6]

The Examiner also rejected Claims 1, 5, 7 and 11 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,033,956 ("Wu"). The Examiner states:

> [6.] Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 (CVD oxide, inherently shows the oxide is the high temperature oxide) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (inherently shows the insulator layer forming sidewalls around the floating gate to prevent charge leaking from the floating gate, see fig. 2C), wherein the insulator layer is directly on the floating gate; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

Claims 1 & 7

Wu does not disclose depositing an insulator layer of high temperature oxide. Claim 1 recites, in part, "depositing an insulator layer of high temperature oxide." Similarly, Claim 7 recites, in part, "depositing an insulator layer of high temperature oxide." Additionally, both Claims 1 and 7 recite "wherein the insulator layer of high temperature oxide is formed by a LPCVD process."

Wu, on the other hand, discloses a "conformal CVD TEOS (tetraethyl orthosilicate) oxide 210" rather than a high temperature oxide formed by a LPCVD process. A conformal

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CVD TEOS oxide is not formed by a LPCVD process. Thus, Wu fails to anticipate Claims 1 and 7.

As the Examiner himself admits, Wu fails to disclose the invention, therefore, the § 102(e) rejection based on Wu is inappropriate. As the Examiner previously recognized and even restates in the present Office Action, Wu fails to disclose all of the elements of the present invention. In the Office Action dated February 12, 2002, and in the present Office Action, the Examiner states that "Wu discloses the claimed invention **except** LPCVD oxide." (Emphasis added; OA, page 5, paragraph 8.) Hence, the § 102(e) rejection is not appropriate. Reconsideration and withdrawal of this rejection of independent Claims 1 and 7 are thus requested.

Claims 5 & 11

Claims 5 and 11 depend on independent Claims 1 and 7 respectively. For the same reasons of allowability as pertain to independent Claims 1 and 7, dependent Claims 5 and 11 are also allowable. Reconsideration and allowance of dependent Claims 5 and 1 are thus requested.

V. 35 U.S.C. § 103 -- Claim Rejections [OA ¶¶ 7-8]

The Examiner rejected dependent Claims 21-22 and independent Claim 23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,033,956 ("Wu"). The Examiner states:

> [8.] Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 (not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.

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Wu discloses the claimed invention except LPCVD oxide; the subject matter as a whole having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

Claims 21 & 22

The features of Claims 21 and 22 are presently incorporated into independent Claims 1 and 7, respectively. Claims 21 and 22 are cancelled. As shown above, independent Claims 1 and 7 are allowable.

Furthermore, the structure disclosed in Wu does not meet Claims 1 and 7. That is, Claims 1 and 7 are directed to "making a flash memory cell." Wu, however, addresses "forming contactless array for high density ROM," and in particular, addresses the "fabrication of SPEAR FAMOS devices. A SPEAR FAMOS device is a Self-aligned Planar EPROM Array Floating gate Avalanche injection MOS.

In addition, the Examiner misconstrues the Claims and Specification. The Examiner stated "on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results." The Specification actually states "Alternatively, other insulator materials, ... can also be used, **if** floating gate undergoes the optional thermal oxidation described above to seal side surfaces 17. (Specification, page 4, lines 24-27; Emphasis added.) The present Claims do not call for the optional thermal oxidation, therefore it is **incorrect** to interpret the Specification as stating that "any other dielectric material will provide the same results." **Again, the Examiner miscontrues the Claims and Specification.** The Examiner states "In addition, the disclosure fails to mention the criticality of the LPCVD process." On the contrary, the Specification clearly states that "Insulator 30 is preferably a high quality oxide which will **prevent charge from leaking out vertical side surfaces 17 of floating gate 16.** High temperature oxides, such as **a LPCVD furnace grown oxide**, are high quality oxides." (Specification, page 4, lines 22-24.)

Reconsideration and allowance of Claims 1 and 7 are thus requested.

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Claim 23

The Examiner also rejects Claim 23. Claim 23 recites, in part, "the insulator layer **forming sidewalls of high quality oxide around the floating gate** to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by LPCVD process." (Emphasis added.) Again, as stated above, Wu does not disclose using a high quality oxide. For the reasons explained above for the patentability of independent Claim 1, independent Claim 23 is similarly allowable.

Reconsideration and withdrawal of the above rejection are thus requested.

VI. 35 U.S.C. § 103 -- Claim Rejections [OA ¶ 9]

The Examiner rejected dependent Claims 3, 4, 6, 9, 10, 12, 14, 15, 21 and 22 and independent Claim 23 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,033,956 ("Wu") or U.S. Patent 4,713,142 ("Mitchell") taken with U.S. Patent 4,613,956 ("Paterson") in view of U.S Patent 5,808,339 ("Yamagishi") and the "applicant's admitted prior art." The Examiner states:

> [9.] Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204; depositing an insulator layer of oxide 210 (not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, **applicant discloses that any other dielectric material will provide the same results.** In addition, **the disclosure fails to mention the criticality of the LPCVD process**) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G, cols. 1-6.
>
> Mitchell et al. discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 32 formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 33 (fig. 2a); depositing an insulator layer of oxide 37 (not limited to any particular type CVD methods [i.e., LPCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, **applicant discloses that any other dielectric material will provide the same results**. In addition, **the disclosure fails to mention the**

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criticality of the LPCVD process) on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c); polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d); and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-5, cols. 1-6.

Again, the Examiner misconstrues the Claims and Specification. The Examiner is incorrect in stating that "any other dielectric material will provide the same result." As stated earlier, the specification actually states "Alternatively, other insulator materials, ... can also be used, **if** floating gate undergoes the optional thermal oxidation described above to seal side surfaces 17. (Specification, page 4, lines 24-27; Emphasis added.) The present Claims do not call for the optional thermal oxidation, therefore it is **incorrect** to interpret the Specification as stating that "any other dielectric material will provide the same results."

Additionally, the Examiner misconstrues the Claims and Specification again when stating the disclosure fails to mention the criticality of the LPCVD process." On the contrary, the Specification clearly states that "Insulator 30 is preferably a high quality oxide which will **prevent charge from leaking out vertical side surfaces 17 of floating gate 16.** High temperature oxides, such as **a LPCVD furnace grown oxide**, are high quality oxides." (Specification, page 4, lines 22-24.)

Claims 3, 4, 6, 9, 10, 12, 14, 15, 21 & 22

Claims 3, 4 and 6, are dependent on independent Claim 1. Claims 9, 10, 12, 14, 15 are dependent on independent Claim 7. Cancelled Claims 21 and 22 are presently cancelled. As shown above, independent Claims 1 and 7 are allowable. Being dependent on allowable Claims, dependent Claims 3, 4, 6, 9, 10, 12, 14 and 15 are also allowable.

Claim 23

The Examiner further states:

> Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Wu or Mitchell et al. with the teaching of Paterson et al. and Yamagishi et al. and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device. **In addition, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made**

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to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for any particular purpose and it appears that the invention would perform equally well with any CVD processes.

(Emphasis added.)

Claim 23 recites, in part:

> depositing an insulator layer of high quality oxide on the tunnel oxide and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming sidewalls of high quality oxide around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by LPCVD process

For the reasons explained above for the allowance of independent Claims 1 and 7, independent Claim 23 is also allowable. (See *supra*, Section III re: MITCHELL.) Additionally, the selection of a "LPCVD process" is not simply a "design choice" as stated by the Examiner and the Examiner provided no support for this assertion in the prior art. The LPCVD process is selected for the reasons stated in the Specification on page 4, lines 22-27, that is, to "prevent charge from leaking out from the vertical side surfaces 17 of the floating gate."

Reconsideration and withdrawal of this rejection are thus requested.

VII. 35 U.S.C. § 103 -- Claim Rejections [OA ¶ 10]

The Examiner rejected Claims 1, 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15, 21, 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over U.S Patent 5,808,339 ("Yamagishi") or U.S. Patent 6,051,467 ("Chan") taken with Sze et al., "ULSI Technology" ("Sze") in view of "Applicant's admitted prior art."

The Examiner improperly combines the references. MPEP § 2143 provides:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

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The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.[2] In particular, because none of the cited references suggests or discloses a "high temperature oxide" or an LPCVD process for forming a single oxide layer over a floating gate that can act to both insulate the floating gate and prevent charges from leaking, the Examiner combination of Sze and the cited references can only be made by hindsight. Obviousness may not be established by hindsight reconstruction or conjecture.[3]

If the Examiner disagrees, Applicants respectfully request that the Examiner point out the suggestion or motivation to combine the cited references with more specificity in support of this § 103 rejection, as required under MPEP § 2143.01 and § 2143.03. A prima facie case of obviousness not being established, it is respectfully requested that § 103 rejection to be withdrawn.

Reconsideration and allowance of the pending Claims are thus requested.

Independent Claims 1, 7 and 23

With reference to the deficiencies of Yamagishi and Chan, the Examiner states:

> [10.] Yamagishi et al. (figs. 9A-lOD) discloses ... depositing an insulator layer of oxide 54 (by CVD) on the substrate and the floating gate ...
>
> Chan et al. further discloses a method ... depositing an insulator layer of oxide 30 (by CVD methods, Le, APCVD or PECVD) on the substrate and the floating gate ...
>
> However, the above references do not explicitly shows forming high temperature oxide by using LPCVD method (Note: during the telephone interview dated on 8/3/2001, applicant admitted that this layer is well known in the art and it is formed by LPCVD process, also see the amendment dated on 8/6/2001, **furthermore, applicant stated in the specification, other dielectric may used, i.e., see page 3, lines 26-30. In addition, the disclosure fails to mention the criticality of the LPCVD process).**

(Emphasis added.)

Again, the **Examiner misconstrues the Specification** and Claims. The Examiner is incorrect in stating that "other dielectric [material] may [be] used." As stated earlier, the specification actually states "Alternatively, other insulator materials, ... can also be used, **if**

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[2] In re Mills, 916 F.2d 680 (Fed. Cir. 1990).
[3] ACS Hospital Systems, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984).

floating gate undergoes the optional thermal oxidation described above to seal side surfaces 17. (Specification, page 4, lines 24-27; Emphasis added.) The present Claims do not call for the optional thermal oxidation, therefore it is **incorrect** to interpret the Specification as stating that "any other dielectric material will provide the same results."

The Examiner also states that:

> It is well known in the art to form the dielectric by using any CVD process. For example, **Sze et al. teaches forming the dielectric by using LPCVD process**, such will provide excellent purity and uniformity, confomal [*sic*] step coverage, large wafer capacity, high throughput, etc. Furthermore, it is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, **applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate**, see pages 1-2.
>
> (Emphasis added.)

The "dielectric layer" is not the "insulator layer." It appears the Examiner is equating the dielectric layer and the insulator layer. Claim 1 recites both "depositing an **insulator layer** of high temperature oxide" and "depositing a **dielectric layer** on the planar surface directly over the exposed top surface of the floating gate and the **insulator layer**." Claim 1 also recites that "the **insulator layer** of high temperature oxide is formed by a LPCVD process." The Examiner states that "Sze et al. teaches forming the dielectric by using LPCVD process" and that "applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate." Both references by the Examiner are directed to the dielectric and not the insulator. It is believed that neither Sze nor the Applicant's admitted prior art shows an "**insulator layer** of high temperature oxide is formed by a LPCVD process."

The Examiner also states:

> Furthermore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the standard process of Yamagishi et al. or Chan et al. with the teaching of Sze et al. and Applicant's admitted prior art because of the desirability to improve device reliability and performance of the device (also see above); in addition, **the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as matter of design choice since applicant has not disclosed that LPCVD method solves any stated problems or is for**

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any particular purpose and <u>it appears that the invention would perform equally well with any CVD processes</u>.

(Emphasis added.)

The Examiner again misconstrues the Claims and Specification. The Examiner stated "it appears that the invention would perform equally well with any CVD processes." The Specification actually states "Alternatively, other insulator materials, ... can also be used, **<u>if</u>** floating gate undergoes the optional thermal oxidation described above to seal side surfaces 17. (Specification, page 4, lines 24-27; Emphasis added.) The present independent Claims do not call for the optional thermal oxidation, therefore it is **<u>incorrect</u>** to interpret the Specification as stating that "the invention would perform equally well with any CVD processes."

Reconsideration and allowance of Claims 1, 7 and 23 are thus requested.

<u>Dependent Claims 3 and 9</u>

The Examiner also states:

> Furthermore, the thickness of claims 3 and 9 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. ...

Claims 3 and 9 depend from independent Claims 1 and 7 respectively. For at least the reasons shown above for the allowability of Claims 1 and 7, dependent Claims 3 and 9 are also allowable.

<u>Claims 4, 5, 6, 9, 10, 11, 12, 14 & 15</u>

Claims 4, 5 and 6 depend on Claim 1. Claims 9, 10, 11, 12, 14 and 15 depend on Claim 7. For at least the reasons shown above for the allowability of Claims 1 and 7, dependent Claims 4, 5 and 6 are also allowable.

<u>Claims 21 & 22</u>

Claims 21 and 22 are presently cancelled and their content incorporated into independent Claims 1 and 7, respectively.

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Reconsideration and allowance of the pending Claims are thus requested.

CONCLUSION

After considering this Response, the Examiner is respectfully requested to find this application in condition for allowance. If there are any questions regarding this application, please call the undersigned at (408) 453-9200.

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Version with markings to show changes made.

The following provides a marked up version of the amended claims containing the newly introduced changes. Additions are underlined and deletions are [bracketed]. Claims 1, 7 and 23 are presently amended.

1. (Four Times Amended) A method of making a flash memory cell including a substrate and a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer of high temperature oxide directly on [the substrate] exposed portions of the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer forming [sidewalls] around vertical surfaces of the floating gate to prevent charge leaking from the floating gate, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

7. (Five Times Amended) A method of making a flash memory cell having a substrate and a tunnel oxide layer formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer of high temperature oxide directly on exposed portions of the tunnel oxide layer and the floating gate such that the insulator layer has a thickness that is greater than the first thickness, and wherein the insulator layer of high temperature oxide is formed by a LPCVD process;

polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

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23. (Twice Amended) A method of making a flash memory cell including a substrate, a tunnel oxide layer formed on the substrate and a floating gate, the method comprising:

depositing an insulator layer of high quality oxide on the tunnel oxide layer and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and the insulator layer [forming sidewalls] of high quality oxide on the vertical surfaces around the floating gate to prevent charge leaking from the floating gate, wherein the high quality oxide is formed by a LPCVD process;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface over the exposed top surface of the floating gate and the insulator layer.

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